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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,662	07/27/2004	Jui-Tsen Huang	12336-US-PA	4661

31561 7590 08/08/2007  
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE  
7 FLOOR-1, NO. 100  
ROOSEVELT ROAD, SECTION 2  
TAIPEI, 100  
TAIWAN

EXAMINER
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HARRISON, MONICA D

ART UNIT	PAPER NUMBER
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2813

NOTIFICATION DATE	DELIVERY MODE
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08/08/2007

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

<b>Office Action Summary</b>	Application No. 10/710,662	Applicant(s) HUANG, JUI-TSEN	
	Examiner Monica D. Harrison	Art Unit 2813	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 July 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 9, 11-14 and 19 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8, 10, 15, 16, 18 and 20 is/are rejected.
- 7) ☒ Claim(s) 17 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |                                                                                      |                                                                   |
|--------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____                                                          | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

1. Applicant's request for continued examination (RCE) filed 7/23/07 has been entered. Examiner acknowledges claims 9, 11-14 and 19 are cancelled.

#### ***Claim Objections***

2. Claim 17 is objected to because of the following informalities: Claim 17 depends from cancelled claim 9. Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 10, 15, 16, 18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Chakravorty (6,181,569 B1).

3. Regarding claim 1, Chakravorty discloses a stress relieving method for a wafer, comprising the steps of: providing a wafer (Figure 4, reference 301) with a dielectric layer thereon (Figure 4, reference 305), wherein the wafer is divided into a first area (Figure 5, reference 304) and a second area (Figure 5, reference 305) such that at least no circuits are formed on the dielectric layer within the first area (Figure 5, reference 305); forming a plurality of first openings in the dielectric layer within the first area (Figure 5, above reference 304); and forming a first material layer over the wafer, wherein the upper surface of the first material layer has pits at locations over the first openings and the first material layer is a high stress dielectric layer (Figure 5, reference 308).

4. Regarding claim 2, Chakravorty discloses wherein the first area comprises a scribe line (Figure 6, reference 303).
5. Regarding claim 3, Chakravorty discloses wherein the second area comprises a region for forming a die (Figure 5a, reference 302).
6. Regarding claim 4, Chakravorty discloses wherein the first area comprises a scribe line (Figure 6, reference 303).
7. Regarding claim 5, Chakravorty discloses wherein the first area and the second area are both regions for forming a die (Figure 5a).
8. Regarding claim 6, Chakravorty discloses wherein the step of forming first openings in the dielectric layer within the first area further comprises forming a plurality of second openings in the first dielectric layer within the second area at the same time and then depositing material into the second openings to form a plurality of second material layers (Figure 5a).
9. Regarding claim 7, Chakravorty discloses wherein the first opening is not deep enough to expose film layer underneath the dielectric layer (Figure 5a, above reference 304).
10. Regarding claim 8, Chakravorty discloses wherein the first opening exposes a film layer underneath the dielectric layer (Figure 5a).
11. Regarding claim 10, Chakravorty discloses a stress relieving method for a wafer, comprising the steps of: providing a wafer (Figure 1, reference 301) with a dielectric layer thereon (Figure 4, reference 305), wherein the wafer is divided into a first area and a second area such that no circuits are formed within the first area (Figure 4, underneath reference 305), the first area comprising a scribe line (Figure 6, reference 303), the second area comprising a region

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for forming a die (Figure 5a, reference 302) wherein there is no opening formed in the dielectric layer within the first area (Figure 5a, reference 305); forming a first material layer over the wafer to cover the dielectric layer (Figure 5, reference 308); and forming a plurality of first openings in the first material layer within the first area (Figure 5a, above reference 10).

12. Regarding claim 15, Chakravorty discloses wherein the first opening is not deep enough to expose the dielectric layer (Figure 4, above reference 304). 1

13. Regarding claim 16, Chakravorty discloses wherein the first opening exposes the dielectric layer (Figure 4, reference 305).

14. Regarding claim 18, Chakravorty discloses wherein the first material layer is fabricated from a dielectric material or a metal material (Figure 5, reference 308).

15. Regarding claim 20, Chakravorty discloses wherein the first material layer is a high stress dielectric layer (Figure 5, reference 308).

### ***Response to Arguments***

16. Applicant's arguments with respect to claims 1-8, 10, 15-18 and 20 have been considered but are moot in view of the new ground(s) of rejection. Examiner also notes that there is no mention of a high-k film in the specification nor the examples given in the arguments. Also, for a layer to be a highly stressed, it must have discontinuity or breaks within the layer. Layer 308 has discontinuity which makes it a high stress layer.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Monica D. Harrison  
AU 2813

mdh  
July 31, 2007



MICHAEL LEBENTRITT  
SUPERVISORY PATENT EXAMINER